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(71)Applicant : MITSUBISHI ELECTRIC CORP

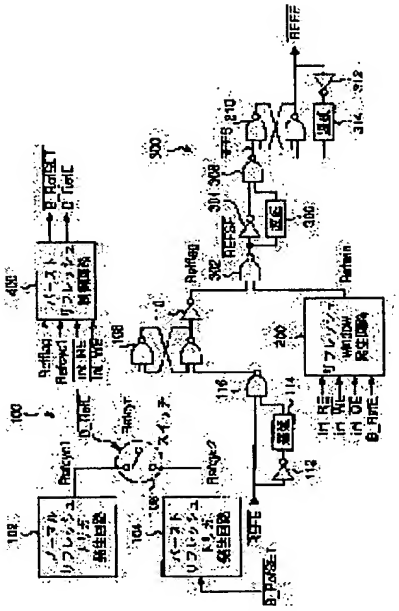
(72)Inventor : TSUKIDE MASAKI

(54) SEMICONDUCTOR MEMORY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To secure stability of refresh-operation in a semiconductor memory device provided with a memory cell array including a plurality of memory cells arranged in a matrix state.

SOLUTION: A refresh control circuit refreshing data held by a plurality of memory cells without externally instructed is provided with a refresh-cycle generation circuit generating first and second refresh-cycles, when refresh operation is not performed in a longer period than a first refresh-cycle time generated by the first refresh-cycle generation circuit, a refresh-execution circuit performs continuously refresh-operation making the second refresh-cycle generated by the second refresh-cycle generation circuit as a start point in the long period or at finish of the long period.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The operating state which can perform read-out actuation and write-in actuation of data, The memory cell array which is the semiconductor memory which has the standby condition of holding said data, and contains two or more memory cells arranged in the shape of a matrix, It has the refresh control circuit refreshed for the data which said two or more memory cells hold. Said refresh control circuit The 1st refresh cycle generating circuit which generates the 1st refresh cycle, The 2nd refresh cycle generating circuit which generates the 2nd refresh cycle of a period shorter than the 1st refresh cycle time, Refresh actuation will be performed, if refresh actuation is attained after the 1st refresh cycle is generated by the 1st refresh cycle generating circuit. And when period refresh actuation longer than the 1st refresh cycle time generated by the 1st refresh cycle generating circuit has not been carried out, The semiconductor memory characterized by having the refresh activation circuit which carries out refresh actuation continuously based on the 2nd refresh cycle generated by the 2nd refresh cycle generating circuit at the time within the long period of termination of the long period.
[Claim 2] The aforementioned refresh activation circuit is the semiconductor memory indicated by claim 1 characterized by having the detecting circuit which detects having not carried out period refresh actuation still longer than the 1st refresh cycle time.
[Claim 3] The semiconductor memory indicated by claim 2 characterized by detecting it as it being the aforementioned long period when it has the counter with which the aforementioned detecting circuit counts the 1st refresh cycle in the condition that refresh actuation is demanded and a counter counts the 1st refresh cycle more than the count of predetermined.
[Claim 4] The aforementioned semiconductor memory is a semiconductor memory with which internal low system actuation of a memory cell array is started in response to an external output enable signal or an external write enable signal. As for the aforementioned refresh activation circuit, a period active state with long external output enable signal or external write enable signal continues. When period refresh actuation longer than the 1st refresh cycle time generated by the 1st refresh cycle generating circuit has not been carried out, An external output enable signal or an external write enable signal will be in a non-active state. At the period when internal low system actuation becomes non-activity The semiconductor memory indicated by either claim 1 characterized by summarizing the refresh actuation based on the 1st refresh cycle by **********, and carrying out refresh actuation based on the 2nd refresh cycle - claim 3.
[Claim 5] The aforementioned 2nd refresh cycle generating circuit is the semiconductor memory indicated by either claim 1 characterized by generating the 2nd refresh cycle when period refresh actuation longer than the 1st refresh cycle time generated by the 1st refresh cycle generating circuit has not been carried out, and refresh actuation is carried out - claim 3.
[Claim 6] The aforementioned semiconductor memory is a semiconductor memory with which internal low system actuation of a memory cell array is started in response to external address change. The aforementioned refresh activation circuit When period refresh actuation longer than the 1st refresh cycle time which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit has not been carried out, An external output enable signal or an external write enable signal will be in a non-active state. At the period when internal low system actuation becomes non-activity The semiconductor memory indicated by either claim 1 characterized by summarizing the refresh actuation based on the 1st refresh cycle by **********, and carrying out refresh actuation based on the 2nd refresh cycle - claim 3.
[Claim 7] The aforementioned refresh activation circuit is the semiconductor memory indicated by claim

6 characterized by stopping internal low system actuation, when period refresh actuation longer than the 1st refresh cycle time which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit has not been carried out and an external output enable signal or an external write enable signal will be in a non-active state.

[Claim 8] As for the aforementioned refresh activation circuit, the condition that the address does not change continues. If it will be in an external output enable signal or a write enable signal non-active state when period refresh actuation longer than the 1st refresh cycle time generated by the 1st refresh cycle generating circuit has not been carried out The semiconductor memory indicated by claim 6 which summarizes the refresh actuation based on the 1st refresh cycle by **********, carries out refresh actuation based on the 2nd refresh cycle, and is characterized by the thing [carrying out re-activity of the low system based on this, after ending by the count].

[Claim 9] The aforementioned refresh activation circuit is the semiconductor memory indicated by claim 4 or claim 6 characterized by not carrying out when an external output enable signal or an external write enable signal is activated after inactivation more quickly than a predetermined period while activating the aforementioned refresh actuation collectively carried out based on the 2nd refresh cycle after inactivation of an external output enable signal or a write enable signal.

[Claim 10] The aforementioned semiconductor memory is a semiconductor memory with which the interior low system actuation of a memory cell array is started in response to external address change. The aforementioned refresh activation circuit When the condition that the address is long and of not carrying out period change continues, after the condition has been recognized, it carries out based on the next address change. The semiconductor memory indicated by either claim 1 characterized by summarizing the refresh actuation based on the 1st refresh cycle by **********, and carrying out refresh actuation based on the 2nd refresh cycle - claim 3.

[Claim 11] The aforementioned semiconductor memory is a semiconductor memory with which internal low system actuation of a memory cell array is started in response to external address change. The aforementioned refresh activation circuit When period refresh actuation longer than the 1st refresh cycle time which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit has not been carried out, Make low system actuation deactivate, summarize the refresh actuation based on the 1st refresh cycle by **********, and refresh actuation is carried out based on the 2nd refresh cycle. The semiconductor memory indicated by either claim 1 characterized by reactivating low system actuation after ending the refresh actuation for the count furthermore - claim 3.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor memory which it is not dependent on an input signal from the outside, and can perform refresh actuation in more detail about a semiconductor memory.
[0002]
[Description of the Prior Art] In personal digital assistants, such as a cellular phone, the general purpose static mold semiconductor memory (SRAM is called hereafter) asynchronous [without the need for supply of an external clock] is adopted widely. Since refresh actuation is unnecessary, the complicated control of the control for which it waits until a refresh cycle ends access of MEMORIHE under refresh actuation of SRAM is unnecessary. Therefore, when using SRAM, simplification of a system configuration is possible and SRAM was suitable for use with a personal digital assistant.
[0003] However, in recent years, the function of a personal digital assistant is improving sharply and the memory function of large capacity [personal digital assistant] is needed. If the memory cell size of SRAM becomes a bulk memory from a certain thing by SRAM about 10 times as compared with the memory cell size of a dynamic mold semiconductor memory (DRAM is called hereafter), the price of a chip will rise sharply, consequently the price of a personal digital assistant will rise. Therefore, the idea to which the cost per unit bit of memory uses low DRAM for a personal digital assistant instead of SRAM has been born.
[0004] DRAM has the operating state which can perform read-out and the store of data, and the standby condition of holding data, and needs to maintain a storage condition by refresh actuation. Therefore, complicatedly [to be memory controlled] of DRAM for performing refresh actuation. Therefore, it is not easy to adopt DRAM as an alternate memory of SRAM for the personal digital assistant manufacturer who has designed the system by using SRAM as memory until now.
[0005] For this reason, although the memory itself was DRAM, development of the new semiconductor memory which operates as SRAM externally began to be performed briskly [each chip makers]. This new semiconductor memory is reported by KAZUHIRO SAWADA et al., IEEE J0URNAL 0 F SOLID-STATE CIRCUITS, VOL.23, N0, 1, FEBRUARY 1998, and p12-19.
[0006] What has an internal memory cell the same as the memory cell in DRAM is used for this new semiconductor memory. External interfaces inputted into this semiconductor memory on the other hand, such as a control signal and an address signal, are almost the same as SRAM. Moreover, refresh actuation of this semiconductor memory is not controlled by the signal from the outside like refresh actuation of the conventional DRAM, or self refresh actuation, and is performed based on the refresh activation signal periodically outputted from the refresh circuit inside a semiconductor memory. It is not dependent on an input signal from the outside, and the new semiconductor memory explained above can perform refresh actuation, and is called DRAM with a perfect HIDOUN refresh function based on the function. ("HIDOUN" is semantics that it was hidden from the exterior.) A refresh circuit answers the cycle signal periodically outputted by the timer circuit including the timer circuit which is a ring oscillator, and outputs a refresh activation signal. Since a timer circuit always outputs a cycle signal, as for this new DRAM, refresh actuation is periodically performed in a standby condition also at the time of the operating state which can perform read-out actuation or write-in actuation. By development of this DRAM with a perfect HIDOUN refresh function, the correspondence to advanced features of a personal digital assistant is possible.
[0007]

[Problem(s) to be Solved by the Invention] However, in this DRAM with a perfect HIDOUN refresh function, since refresh actuation was carried out also in the state of operating state or standby, when the demand signal of a refresh activation signal, a store, or read-out actuation is activated to the same timing, malfunction is caused. This is explained below.

[0008] Drawing 19 is a timing chart in case malfunction takes place by DRAM with a perfect HIDOUN refresh function. A chip enable signal / CE is control signals inputted from the outside. (Notation/attached before the notation expresses a negative logic signal with the following explanation.) When a chip enable signal / CE is active states, DRAM will be in operating state, and when a chip enable signal / CE is non-active states, DRAM will be in a standby condition. In the timing chart shown in drawing 19 , till time of day t4, since a chip enable signal / CE is non-active states (H level), DRAM is in the standby condition. In a standby condition, at time of day t1 and t3, activation of a refresh cycle signal / Refcyc is answered, a refresh activation signal / REFE is activated, and refresh actuation is performed. On the other hand, at the time of day t2 whose refresh cycle signal / Refcyc are non-active states, since a refresh activation signal / REFE is non-active states, refresh actuation is not carried out. Then, when a chip enable signal / CE will be in an active state (L level) at time of day t4, DRAM will be in operating state. Therefore, like time of day t5, when a refresh activation signal / REFE is activated, the case where the signal which requires a store or read-out actuation is inputted arises from the exterior. In such a case, DRAM malfunctions.

[0009] In order to prevent generating of such malfunction, the conventional DRAM with a perfect HIDOUN refresh function is installing the Arbitration circuit. An Arbitration circuit is a circuit which compares the demand signal of the store inputted from the refresh activation signal / REFE which is a synchronizing signal, and the outside, or read-out actuation, and adjusts the sequence of operation. When the demand signal of a refresh activation signal / REFE, a store, or read-out actuation is activated to the same timing, specifically, an Arbitration circuit is adjusted so that actuation of the signal activated more quickly may be performed previously and actuation of the signal of another side may be performed after that. Even when the demand signal of a refresh activation signal / REFE, a store, or read-out actuation is activated to the same timing by this, malfunction of DRAM can be prevented to some extent.

[0010] However, when it adjusts so that an Arbitration circuit may carry out store or read-out actuation after refresh actuation, the probability for an access rate to be long overdue becomes high. When the demand signal of a refresh activation signal / REFE, a store, or read-out actuation is activated to the completely same timing, it becomes impossible moreover, to adjust in an Arbitration circuit.

[0011] It is difficult to secure the stability of refresh actuation by the conventional DRAM with a perfect HIDOUN refresh function by the above trouble.

[0012] The purpose of this invention is securing the stability of refresh actuation in the semiconductor memory which has the operating state which can perform read-out and the store of data, and the standby condition of holding data.

[0013]

[Means for Solving the Problem] The semiconductor memory concerning this invention is a semiconductor memory which has the operating state which can perform read-out actuation and write-in actuation of data, and the standby condition of holding said data, and is equipped with the memory cell array containing two or more memory cells arranged in the shape of a matrix, and the refresh control circuit refreshed for the data which said two or more memory cells hold, without being ordered from the outside. The 1st refresh cycle generating circuit where a refresh control circuit generates the 1st refresh cycle, The 2nd refresh cycle generating circuit which generates the 2nd refresh cycle of a period shorter than the 1st refresh cycle time, It has a refresh activation circuit. A refresh activation circuit Refresh actuation will be performed, if refresh actuation is attained after the 1st refresh cycle is generated by the 1st refresh cycle generating circuit. And when period refresh actuation longer than the 1st refresh cycle time generated by the 1st refresh cycle generating circuit has not been carried out, It collects at the time within the long period of termination of the long period, and refresh actuation is continuously carried out based on the 2nd refresh cycle generated by the 2nd refresh cycle generating circuit.

[0014] In the aforementioned semiconductor memory, the aforementioned refresh activation circuit is preferably equipped with the detecting circuit which detects having not carried out period refresh actuation still longer than the 1st refresh cycle time. Preferably, it is detected as the aforementioned detecting circuit being the aforementioned long period, when it has the counter which counts the 1st refresh cycle in the condition that refresh actuation is demanded and a counter counts the 1st refresh cycle more than the count of predetermined.

[0015] The aforementioned semiconductor memory is a semiconductor memory with which the interior low system actuation of a memory cell array is started in response to an external output enable signal or

an external write enable signal. As for a refresh activation circuit, a period active state with long external output enable signal or external write enable signal continues. When period refresh actuation longer than the 1st refresh cycle time generated by the 1st refresh cycle generating circuit has not been carried out, An external output enable signal or an external write enable signal will be in a non-active state. The refresh actuation based on the 1st refresh cycle is summarized by **********, and refresh actuation is carried out based on the 2nd refresh cycle at the period when internal low system actuation becomes non-activity.

[0016] In the aforementioned semiconductor memory, preferably, when an external output enable signal or an external write enable signal is activated after inactivation more quickly than a predetermined period, a refresh activation circuit is not carried out, while activating the aforementioned refresh actuation collectively carried out based on the 2nd refresh cycle after inactivation of an external output enable signal or a write enable signal.
[0017] The aforementioned 2nd refresh cycle generating circuit generates a refresh cycle, when period refresh actuation longer than the 1st refresh cycle time generated by for example, the 1st refresh cycle generating circuit has not been carried out, and refresh actuation is carried out.
[0018] The aforementioned semiconductor memory is a semiconductor memory with which internal low system actuation of a memory cell array is started for example, in response to external address change. A refresh activation circuit When period refresh actuation longer than the 1st refresh cycle time which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit has not been carried out, An external output enable signal or an external write enable signal will be in a non-active state. The refresh actuation based on the 1st refresh cycle is summarized by **********, and refresh actuation is carried out based on the 2nd refresh cycle at the period when internal low system actuation becomes non-activity.
[0019] In the aforementioned semiconductor memory, preferably, the condition that the address does not change continues, and a refresh activation circuit will stop internal low system actuation, if an external output enable signal or an external write enable signal will be in a non-active state when period refresh actuation longer than the 1st refresh cycle time generated by the 1st refresh cycle generating circuit has not been carried out.
[0020] In the aforementioned semiconductor memory preferably When the refresh activation circuit has not carried out period refresh actuation longer than the 1st refresh cycle which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit, If an external output enable signal or an external write enable signal will be in a non-active state After summarizing the refresh actuation based on the 1st refresh cycle by **********, carrying out refresh actuation based on the 2nd refresh cycle and ending by the count, re-activity of the low system actuation is carried out based on this.
[0021] In the aforementioned semiconductor memory, preferably, when an external output enable signal or an external write enable signal is activated after inactivation more quickly than a predetermined period, a refresh activation circuit does not carry out the aforementioned refresh actuation, while the aforementioned refresh actuation collectively carried out based on the 2nd refresh cycle is activated after inactivation of an external output enable signal or a write enable signal.
[0022] The aforementioned semiconductor memory is a semiconductor memory with which internal low system actuation of a memory cell array is started for example, in response to external address change, and when the condition that the address is long and of not carrying out period change continues, after the condition has been recognized, a refresh activation circuit summarizes the refresh actuation based on the 1st refresh cycle by ********** based on the next address change, and carries out refresh actuation based on the 2nd refresh cycle.
[0023] The aforementioned semiconductor memory is a semiconductor memory with which internal low system actuation of a memory cell array is started in response to external address change, and when an external output-enable signal or an external write-enable signal is activated after inactivation more quickly than a predetermined period, a refresh activation circuit is not carried out while activating the aforementioned refresh actuation collectively carried out based on the 2nd refresh cycle after inactivation of an external output-enable signal or a write-enable signal.
[0024] The aforementioned semiconductor memory is a semiconductor memory with which internal low system actuation of a memory cell array is started in response to external address change. A refresh activation circuit When period refresh actuation longer than the 1st refresh cycle time which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit has not been carried out, After making low system actuation deactivate, summarizing the refresh actuation

based on the 1st refresh cycle by **********, carrying out refresh actuation based on the 2nd refresh cycle and ending the refresh actuation for the count further, re-activity of the low system actuation is carried out. In addition, the component explained to the above of this invention is combinable as much as possible.

[0025]

[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained with reference to an attached drawing. In addition, in a drawing, the same reference designator shows a same or equivalent thing. In the semiconductor memory which has the operating state which can perform read-out and the store of data, and the standby condition of holding data, writing and read-out of data are performed by operating state to the memory cell array containing two or more memory cells arranged in the shape of a matrix. A memory cell is the same as the memory cell in DRAM, and needs refresh actuation to a memory cell. Inside a semiconductor device, the clock cycle showing the period for generating a refresh signal is generated, and internal refresh cycle time is prescribed by this clock cycle. The data in a memory cell are held by performing refresh actuation once in internal refresh cycle time. It is not dependent on an input signal from the outside, and this semiconductor memory performs refresh actuation.

[0026] In the semiconductor memory which it is not dependent on an input signal from the outside, and can perform refresh actuation, in order to secure the stability of refresh actuation, this invention person has already proposed performing refresh actuation according to the condition of a semiconductor memory. The condition of a semiconductor memory is, after ending the others and read-out actuation or the write-in actuation at the time of a standby condition. However, there is a problem that storage cannot be operated in the long period (long cycle) beyond internal refresh cycle time (for example, several 10microsec) in this semiconductor memory. Drawing 1 shows one example of the situation that in the case of the semiconductor memory which carries out refresh actuation after implementation of read-out actuation or write-in actuation refresh actuation is not performed in (/CE="L") and a long cycle when a chip is enabling. In this example, read-out or a write-in condition continues in the period longer than internal refresh-cycle-time tref, and refresh actuation is not performed in the meantime. Then, although refresh actuation is performed in the standup of refresh period signal Refwin="H", since read-out actuation or write-in actuation is not carried out for a long time, data will be destroyed. Similarly, also with the semiconductor memory of the configuration of the address trigger method which controls the low (Row) system of the memory cell array 26 according to change of the address, if the address has not changed for a long time at the time of /CE="L", since the origin which activates refresh actuation does not exist, data will be destroyed. Therefore, as an external specification, although a limit does not exist in the period of /CE="H", during the period of /CE="L", limit of surely carrying out read-out actuation, write-in actuation, or address change is needed in internal refresh cycle time.

[0027] So, in this invention, actuation is made possible in the semiconductor memory which it is not dependent on an input signal from the outside, and can perform refresh actuation, without a long cycle longer than internal refresh cycle time also destroying data. A refresh control circuit is equipped with the circuit which generates the usual refresh cycle (the 1st), and the circuit which generates the refresh cycle (the 2nd) of a period quicker than it. When it is not a long cycle, refresh actuation is performed based on the 1st refresh cycle (when rapid access is required). On the other hand, when the long cycle beyond internal refresh cycle time comes, in a need period (at inside of a long cycle, or the time of termination), automatically, a refresh control circuit summarizes only the count to which the internal refresh cycle was skipped based on the 2nd refresh cycle, and performs refresh actuation continuously. (Below, this is called burst refresh.) A semiconductor memory can control refresh actuation in this way, without being dependent on an external signal. Therefore, it is not necessary to prepare a limit of an external specification. In addition, although recognition of a long cycle is automatically performed with the gestalt of implementation of the operation explained below, it may recognize a long cycle in the exterior of a semiconductor memory, and may tell a semiconductor device about the result. In this case, a semiconductor memory performs refresh control corresponding to it.

[0028] Gestalt 1. drawing 2 of operation shows the whole semiconductor-memory (DRAM) configuration with the unnecessary external refresh control in the gestalt 1 of implementation of invention. The memory cell array 26 consists of two or more DRAM cels arranged in the shape of a matrix in this semiconductor memory. As external pins 10-16, it has the same control pin as SRAM. The input terminal group 10 which receives the chip enable signal / CE which is a control signal, an output enable signal / OE, a write enable signal / WE, a control signal / LB, and /UB in DRAM, The terminal block 11 by which low order data signal DQ0-DQ7 is outputted and inputted, and the terminal block 12 by which high order data signal

DQ8-DQ15 is outputted and inputted, The terminal block 15 into which train address signal A0-Am (m is the one or more natural numbers) is inputted, The terminal block 16 into which address signal Am+1-An (n is the one or more natural numbers) is inputted, the power supply terminal 13 with which supply voltage VCC is given, and the earth terminal 14 with which the touch-down electrical potential difference GND is given are formed. Unlike the usual DRAM, the address is not time-division system. Refresh actuation is carried out after implementation of read-out actuation or write-in actuation. Furthermore, it has the refresh control circuit 40 which controls refresh actuation without the control from the outside, and refresh actuation is carried out based on the refresh activation signal / REFE which the refresh control circuit 40 outputs. Thereby, the refresh control from the outside becomes unnecessary.

[0029] In DRAM, a control circuit 20 answers the control signal inputted from a terminal block 11, and outputs the control clock equivalent to the predetermined mode of operation of DRAMs, such as a write-in mode of operation and a read-out mode of operation, to each block. When a control signal is explained, a chip enable signal / CE is signals which make DRAM operating state. An output enable signal / OE is a signal which activates an output buffer while setting DRAM as a read-out mode of operation. A write enable signal / WE is signals which set DRAM as a write-in mode of operation. A control signal/LB is signals which choose outputting and inputting data from the data terminal block 11 by the side of a lower bit, and a control signal/UB is signals which choose outputting and inputting data from the data terminal block 12 by the side of a high order bit. In addition, the configuration of a control circuit 20 is the same as that of the conventional DRAM except refresh control.

[0030] The train (column) address buffer 21 is transmitted to the interior in response to address signal A0-Am according to the output of a control circuit 20. The line (low) address buffer 22 is transmitted to the interior in response to address signal Am+1-An according to the output of a control circuit 20. The train decoder 23 receives the internal address signal which the train address buffer 21 outputs according to the output of a control circuit 20, and specifies the train address. The line decoder 24 receives the internal address signal which the line address buffer 22 outputs according to the output of a control circuit 20, and specifies a line address. The memory cell array 26 consists of two or more memory cells arranged in the shape of a matrix. A sense amplifier and the input/output control circuit 25 perform write-in actuation to the memory cell array 26, and amplify the output from the memory cell array 26, and perform read-out actuation.

[0031] Furthermore, the low order input buffer 27 is transmitted to a sense amplifier and the input/output control circuit 25 in response to data signal DQ0-DQ7 according to the output of a control circuit 20 from a terminal block 11. The low order output buffer 28 outputs a data signal to a terminal block 11 in response to the signal from a sense amplifier and the input/output control circuit 25 according to the output of a control circuit 20. The high order input buffer 29 is transmitted to a sense amplifier and the input/output control circuit 25 in response to data signal DQ8-DQ15 according to the output of a control circuit 20 from a terminal block 12. The high order output buffer 30 outputs a data signal to a terminal block 12 in response to the signal from a sense amplifier and the input/output control circuit 25 according to the output of a control circuit 20.

[0032] The refresh control circuit 40 controls refresh actuation without the refresh control from the outside. If the refresh control circuit 40 outputs the refresh activation signal / REFE which is the signal activated periodically to a control circuit 20, a control circuit 20 receives a refresh activation signal / REFE, and in order to carry out refresh actuation, it will output each BUROKKUHE movement directive signal. Below, the refresh control circuit 40 is explained in detail.

[0033] Drawing 3 shows the configuration of the refresh control circuit 40. In the refresh control circuit 40, the refresh flag generating circuit 100 generates the signal (refresh flag Refflag) which shows whether the interior of a chip is demanding refresh actuation. (When the refresh flag Refflag is "H", those with a refresh demand are meant.) The refresh period generating circuit 200 generates the refresh period signal Refwin which shows the period (Window) in which refresh actuation is possible. The circuit 300 which generates a refresh activation signal / REFE generates the refresh activation signal (/REFE) which controls refresh activation from two signals, the refresh flag Refflag and the refresh period signal Refwin. The burst refresh control circuit 400 is recognized to be a long cycle, is a control circuit which controls the burst refresh which summarizes refresh actuation two or more times, and performs it continuously, and generates burst refresh activation signal B_RefE.

[0034] The refresh flag generating circuit 100 is equipped with the Normal refresh trigger generating circuit 102 which considered the ring oscillator which usually sometimes outputs a refresh cycle (signal name: Refcyc1) with a predetermined period as the basic configuration, and the burst refresh trigger generating circuit 104 which generates the refresh cycle (signal name: Refcyc2) when carrying out

continuous refresh actuation (burst refresh) of multiple times at a predetermined stage. A refresh cycle Refcyc1 is equivalent to the refresh cycle (internal refresh cycle time) in the usual DRAM. The burst refresh trigger generating circuit 104 is equipped with a configuration as shown in drawing 4 , and serves as a ring oscillator which turns a short period compared with the period of the usual refresh timer. Moreover, the control function for not oscillating this ring oscillator is added at the time of the modes other than burst refresh (B_RefSET="H"), and low consumerization is attained. A switch 106 chooses the period outputted from one of two refresh trigger circuits 102 and 104. It is controlled by the burst refresh activation signal / B_RefE generated from the burst refresh control circuit 400 which period is chosen. Activation of /B_RefE chooses the period of the 2nd refresh trigger circuit 104. Based on the refresh cycle signal Refcyc chosen by the switch 106, the refresh flag Refflag is generated through a flip-flop 108 and an inverter 110. Moreover, if refresh actuation is completed, let the refresh flag Refflag be non-activity. For this reason, if a refresh activation signal / REFE is no longer taken out, only predetermined time will be overdue and generating of a refresh flag will be suspended. That is, the refresh activation signal / the REFE signal itself, and the signal which let the inverter 112 and the delay circuit 114 pass for the /REFE signal are inputted into NAND gate 116, and a flip-flop 108 is reset with the output.

[0035] The origin of refresh actuation is a time of both the refresh period signals Refwin that show the period in which the refresh flag Refflag and refresh actuation which were set from the refresh cycle signal Refcyc are possible being activated. In the circuit 300 which generates a refresh activation signal / REFE, it is inputted into NAND gate 302, and through the direct inverter 304, the output signal is inputted into NAND gate 308 through a delay circuit 306, and, as for both the flag Refflag set by the refresh flag generating circuit 100 from Refcyc, and Refwin generated from the refresh period generating circuit 300, outputs a refresh start signal / REFS. This signal is outputted as a refresh activation signal / REFE through a flip-flop 310. Refresh actuation is carried out according to the output of a refresh activation signal / REFE. After it is reversed with an inverter 312 and a refresh activation signal / REFE is delayed by part for a refresh actuation period, and the delay circuit 314, it is inputted into a flip-flop 310 and reset after predetermined time.

[0036] In addition, drawing 5 shows the circuit which generates int/RE (or int / OE signal which is int/WE and the internal output enable signal which are an internal write enable signal) which is an internal write enable signal in a control circuit 20. When chip enable signal CD# from the outside and write enable signal RE# (or write enable signal WE#, or an output enable signal /OE#) are "L" level for all, the signal reversed through the inverter is inputted into a NAND gate, and an int/RE (or int/WE, int/OE) signal is generated. A control circuit 20 sends int/RE, int/WE, and an int/OE signal to the refresh control circuit 40.

[0037] Drawing 6 shows the configuration of the burst refresh control circuit 400. The burst refresh control circuit 400 consists of a circuit which roughly divides, carries out automatic detection of the long cycle, and sets burst refresh, and a burst refresh halt circuit which detects that burst refresh was completed. If automatic detection of the former long cycle is explained using the timing diagram of drawing 7 , it will be realized by the principle shown below. As explained previously, the origin of refresh actuation is a time of both the refresh period signals Refwin that show the period in which the refresh flag Refflag and refresh actuation which were set from the refresh cycle Refcyc are possible being activated, and if refresh actuation is completed, it will make Refflag non-activity. It can be recognized as being a long cycle if the usual refresh cycle Refcyc1 counts twice or more since a long cycle is the case where the write-in condition of a period longer than the usual refresh cycle etc. comes. Then, while Refflag is being activated, the reversal signal of Refcyc1 is outputted by (Refflag="H") and the AND gate 402, and it counts with a counter 404. If a counter 404 counts twice or more, since it can be recognized as it being a long cycle, a flip-flop 406 is set in the phase, and a burst refresh set signal / B_RefSET is outputted. And when the signal that the internal signals int/RE or int/WE is not outputted is taken out from the NOR gate 408, it outputs as burst refresh activation signal B_RefE through the OR gate 410 (when it is in a long cycle and is not in the condition of read-out or a store). Thereby, the refresh period signal Refwin is activated and burst refresh is performed. On the other hand, if part refresh actuation which skipped the usual refresh actuation is performed, the burst refresh halt circuit 420 will detect it as burst refresh having been completed, and will output a reset signal to a flip-flop 406.

[0038] As shown in drawing 8 , the burst refresh halt circuit 420 which detects that burst refresh was completed The counter 422 which counts the count of the usual refresh cycle (Refcyc1) at the time of Refflag activity (Refflag="H"), and when burst refresh is started, It has based on the quick refresh cycle Refcyc2 with the counter 424 which counts the count of refresh actuation. The EXOR gate 426 When these two numbers of counts are in agreement, the single shot pulse circuit 428 is started and the stop

signal/B_RefSTOP which stops burst refresh are generated. Thereby, refresh actuation can be collectively carried out at the inside of the part (counted value of a counter 422) which skipped the usual refresh, and a long cycle (when /OE or /WE is not activity), or the time of long cycle termination.
[0039] Drawing 9 shows the configuration of the refresh period generating circuit 200. At the time of int/CE="H", activity of the refresh period signal Refwin is always carried out through the OR gate 202. Moreover, a burst refresh period (/B_RefE="L") activates the refresh period signal Refwin through the OR gate 202 at the time of int/CE="L." Moreover, when both int/RE and int/WE are not activity (output ="H" of the AND gate 204), the refresh period signal Refwin is activated through the AND gate 206 through the predetermined time delay by the delay circuit 208, and the OR gate 202. Thus, the refresh period signal Refwin is activated at the inside of a long cycle, or the time of the termination. Thereby, burst refresh is activated.
[0040] Actuation of the semiconductor memory of circuitry explained above is explained. First, actuation of the refresh control circuit 40 in the case of usually performing refresh actuation in a cycle (cycle shorter than the usual refresh cycle) is explained using drawing 10 . The refresh cycle signal Refcyc1 is outputted with a predetermined period from the Normal refresh trigger generating circuit 102, and the refresh demand signal Refflag is activated by the refresh flag generating circuit 100 based on this. Moreover, the refresh period generating circuit 200 activates the refresh period signal Refwin which shows the period which checks whether the refresh flag is being activated after termination of read-out or write-in actuation from an external signal. Based on the timing which both this Refwin signal and a Refflag signal activate, the refresh control circuit 300 generates a refresh start signal / RefS, and generates a refresh activation signal / REFE based on this. Here, actuation as usual is carried out, without generating Refcyc2, in order that burst refresh activation signal B_RefE may not carry out activity since it is not recognized as a long cycle.
[0041] Next, the case where read-out or a write-in cycle is carried out in a long cycle (cycle longer than the usual refresh cycle) is explained using drawing 11 (when a low system is controlled by /CE="H" by /OE or /WE). If it is detected that Refcyc turns twice or more in the burst refresh control circuit 400 where Refflag is activated and a long cycle is recognized since the refresh period signal Refwin is not activated when /OE or /WE is fixed by long duration"L", thereby, a burst refresh set signal / R_RefSET will be activated. However, in this phase, burst refresh is not carried out, but a burst refresh activation signal / B_RefE carries out activity of it in the phase in which /OE or /WE became "H", and it starts burst refresh. Moreover, the count of Refcyc1 in case Refflag is "H" is counted, and a count is stopped in the phase (read-out or a store is no longer performed) in which /OE or /WE became "H". If a burst refresh activation signal / B_RefE is activated, the period of refresh will be changed into Refcyc2 from Refcyc1, the refresh period signal Refwin will be activated at this time, the count of refresh actuation which /OE or /WE skipped in the period of "H" by short time amount will be summarized synchronizing with this Refcyc2 (period quite shorter than usual Refcyc1), and refresh actuation will be carried out. It can shift to degree cycle, without becoming the usual read-out or write-in actuation, and delaying access, if after that / OE, or /WE is set to "L" since /OE or /WE is carrying out at the period of "H". The problem of the ability not to make it by this operating in the long cycle beyond the internal refresh cycle time Refcyc1 is solved.

[0042] With the gestalt 1 of gestalt 2. implementation of operation, /OE in a long cycle or /WE carries out burst refresh the period of "H", or after termination of a long cycle in the semiconductor memory with which the low system of the memory cell array 26 is controlled by the trigger of external /OE or /WE. This actuation is not cared about at all, even if it is equivalent to carrying out burst refresh actuation and the interior of a semiconductor memory is the signal which shows the time of non-activity instead of the trigger of /OE or /WE, when the low system in a semiconductor memory is non-activity. With the gestalt 2 of operation, burst refresh in a long cycle is realized in the semiconductor memory of the configuration of the address trigger method by which the low system of the memory cell array 26 is controlled according to change of the address.
[0043] When a low system is controlled by the address trigger, the reset signal of a low system occurs in falling of the /ATD signal generated by detecting change of Address ADD, the low system which is a front cycle is reset, the set signal of a low system is generated in the standup of a /ATD signal, and a low system is activated to the address at this time. The signal generated in these two relation is internal RAS signal int/RAS, the low system is being activated in the period of "L" and int/RAS is non-activity in the period of "H". In addition, drawing 12 shows generating of internal RAS signal int/RAS in a control circuit 20. int / RAS signal is generated in the standup of the /ATD signal generated when an address signal changes. A control circuit 20 sends an int/RAS signal to the refresh control circuit 40. The

configuration of the refresh control circuit 40 is fundamentally the same as the refresh control circuit (drawing 3) of the gestalt 1 of operation except for the burst refresh period generating circuit 200. Unlike the circuit of drawing 9 , in the refresh period generating circuit 200, an int/RAS signal is inputted instead of the output of NAND gate 204. The predetermined time refresh flag Refflag is activated by the standup of an int/RAS signal.

[0044] By the activity approach of the refresh period signal Refwin in this address trigger method, if the refresh flag Refflag is activated synchronizing with a refresh cycle Refcyc, with the activity of the refresh period signal Refwin carried out, a refresh activation signal / REFE will be immediately activated based on this at the time of /CE="H", and it will carry out refresh actuation. Moreover, at the time of /CE="L", as shown in the timing chart of drawing 13 , if the refresh period signal Refwin is activated at the short period of the standup of int/RAS and Refflag is activated at this time, refresh actuation will be carried out.

[0045] the case of an address trigger method -- /CE= -- also when the address has not changed for a long time at the time of "L", in order to enable refresh actuation -- the gestalt 1 of operation -- the same -- the burst refresh control circuit 400 -- /CE= -- address change does not come more than an internal refresh cycle at the period of "L" -- automatic detection -- carrying out -- /OE or /WE -- " -- burst refresh is carried out at the period of H". However, when a low system is controlled by the address trigger, OE or a /WE signal is not participating in low control. After the address changes by this, when a low system waits till the period used as non-activity (int/RAS="H"), and carries out burst refresh and the standup of /OE or /WE already occurs before address change, access from address change will be overdue.

[0046] In order to solve this, as shown in the timing chart of drawing 14 When it is recognized as burst refresh being required for a long cycle, (when a burst refresh activation signal / B_RefE is activated) the refresh control circuit 40 Even if it is in a long cycle, with address change, the low system actuation to this address is reset in the standup of /OE or a /WE signal, and burst refresh is started without relation after that (a burst refresh activation signal /B_RefE="L"). Thereby, when the standup of /OE or /WE occurs before address change, improvement in the speed from address change can be attained. Furthermore, with change of the address, if low system actuation is written without relation as non-activity and there is no address change after burst refresh termination, the low system will not operate. Therefore, since the usual /OE or /WE continues without the address changing and the low system is not activated, the memory cell array 26 cannot be accessed. Then, a low system is automatically activated after burst refresh termination. The rapid access of degree cycle is realizable by taking this technique.

[0047] With the gestalt 2 of the operation to DRAM of the configuration of the gestalt 3. address trigger method of operation, if it is a long cycle when external /OE or /WE serves as "H", burst refresh will be performed. Here, only the count of refresh which skipped the period of "H" of /OE or /WE to the long cycle period must carry out burst refresh, and a certain amount of time amount is needed. When a long cycle continues forever, burst refresh must be carried out for every long cycle. However, if it is a sudden long cycle, even if it does not carry out burst refresh, data corruption will not happen.

[0048] So, if the period of "H" of /OE or /WE is short set up to a single-engined long cycle as shown in the timing chart of drawing 15 , even if recognized as burst refresh being required, it will be made not to carry out burst refresh with the gestalt 3 of operation (even if a burst refresh set signal / B_RefSET is activated). That is, after recognition with a long cycle, when external /OE or /WE serves as "H" (non-activity) in a period shorter than a predetermined period, burst refresh is not carried out. In drawing 15 , when recognized as it being a long cycle, a burst refresh set signal / B_RefSET is activated, but since the period of "H" of after that / OE, or /WE is shorter than a predetermined period, a burst refresh set signal / B_RefSET is deactivated in falling of /OE or /WE. If it carries out like this and burst refresh actuation will begin even once, rapid access after a long cycle can be realized without being able to avoid the problem that big access delay occurs and carrying out data corruption, since read/write actuation cannot be performed until burst refresh is completed.

[0049] Here, the configuration of the refresh control circuit 40 is fundamentally the same as the refresh control circuit (drawing 3) of the gestalt 1 of operation except for the burst refresh control circuit 400. In the burst refresh control circuit 400, unlike the circuit of drawing 6 , the output signal outputted from a flip-flop 406 sends a signal/B_RefSET for the period of "H" of /OE or /WE to the OR gate 410, when short as compared with a predetermined period. For this reason, the counter which counts the period of "H" of /OE or /WE with a clock signal is formed, and a comparator compares the counted value of a counter with the threshold corresponding to the aforementioned predetermined period. If counted value is shorter than a predetermined period, a burst refresh activation signal / B_REF will not be made to output to the OR gate 410.

[0050] Although burst refresh will be carried out if gestalt 4. of operation/OE serves as "H", and it is a long cycle, a limit of the external timing of the period of "H" of /OE is conversely needed. So, with the gestalt 4 of operation, as shown in the timing chart of drawing 16 If /OE recognizes it as burst refresh being required in the condition of "L", (if a burst refresh set signal / B_RefSET is activated) Independently [/OE], if a low system is reset based on address change of degree cycle, a burst refresh activity signal / B_RefE will be activated based on this, and burst refresh will be started (if int/RAS starts). In burst refresh, if the count part refresh actuation skipped by the long cycle is completed, int/RAS will be started and the low system to degree cycle will be activated. By synchronizing with change of the address, the limit of the period of /OE="H" after a long cycle becomes unnecessary, and the degree of freedom of external timing goes up the timing included in burst refresh. In addition, the low system of the memory cell array 26 can apply this control also in the semiconductor memory controlled by the trigger of external /OE or /WE also in the semiconductor memory of the configuration of an address trigger method controlled according to change of the address.

[0051] The configuration of the refresh control circuit 40 is fundamentally the same as the refresh control circuit (drawing 3) of the gestalt 1 of operation except for the burst refresh control circuit 400. In the burst refresh control circuit 400, if unlike the circuit of drawing 6 a burst refresh set signal / B_RefSET (output of a flip-flop 406) is activated and int/RAS starts, delivery, a burst refresh activity signal / B_RefE will be activated for a signal to the OR gate 410. For example, /B_RefSET and an int/RAS signal are inputted into the NOR gate, and the output is sent to the OR gate 410.

[0052] With the gestalt 4 of gestalt 5. implementation of operation, after the condition that address change is long and of not carrying out period change having continued and having recognized it as the long cycle, burst refresh was carried out from deactivation of an internal low system. However, since burst refresh will be carried out from degree cycle if it carries out like this, access delay of degree cycle will arise. With the gestalt 5 of operation, in order to solve this, if it is recognized as a long cycle, without waiting for address change, a low system will be automatically deactivated based on this, and the refresh period signal Refwin will be activated. In this case, it is satisfactory the period tref of the usual refresh cycle. Therefore, since the refresh period signal Refwin is activated, the usual refresh actuation is carried out synchronizing with Refcyc (refer to drawing 17). After summarizing the usual refresh actuation by **********, carrying out refresh actuation and completing the refresh actuation for the count, a low system is again activated based on this. By this control, at the time of a long cycle, since refresh actuation is carried out without synchronizing with the standup of /OE, a limit of the period of /OE="H" after a long cycle becomes unnecessary, and the degree of freedom of external timing goes up.

[0053] Drawing 18 shows the configuration of the refresh control circuit 40 which realizes control shown in drawing 17 . In the refresh control circuit 40, the refresh flag generating circuit 100 generates the signal (refresh flag Refflag) which shows whether the interior of a chip is demanding refresh actuation. (When the refresh flag Refflag is "H", those with a refresh demand are meant.) The refresh period generating circuit 200 generates the refresh period signal Refwin which shows the period in which refresh actuation is possible. The circuit 300 which generates a refresh activation signal / REFE generates the signal (/REFE) which controls refresh activation from two signals, the refresh flag Refflag and the refresh period signal Refwin. The burst refresh control circuit 400 is a control circuit which controls the burst refresh which summarizes refresh actuation two or more times, and performs it.

[0054] The refresh flag generating circuit 100 is equipped with the Normal refresh trigger generating circuit 102 which considered the ring oscillator which usually outputs a refresh cycle (signal name: Refcyc1) with a time predetermined period as the basic configuration. Based on the refresh cycle signal Refcyc1, the refresh flag Refflag is generated through a flip-flop 108 and an inverter 110. Moreover, if refresh actuation is completed, let the refresh flag Refflag be non-activity. For this reason, if a refresh activation signal / REFE is no longer taken out, only predetermined time will be overdue and generating of a refresh flag will be suspended. That is, the refresh activation signal / the REFE signal itself, and the signal which let the inverter 112 and the delay circuit 114 pass for the /REFE signal are inputted into NAND gate 116, and a flip-flop 108 is reset with the output.

[0055] In the refresh period generating circuit 200, activity of the refresh period signal Refwin is always carried out through the OR gate 202 at the time of int/CE="H". Moreover, a burst refresh period (/B_RefE="L") activates the refresh period signal Refwin through the OR gate 202 at the time of int/CE="L." Moreover, when int/RAS is not activity, activity of the refresh period signal Refwin is carried out through the AND gate 206 through the predetermined time delay by the delay circuit 208, and the OR gate 202. Thereby, burst refresh is carried out synchronizing with the quick refresh cycle Refcyc2.

[0056] The origin of refresh actuation is a time of both the refresh flags Refflag and refresh period signals

Refwin that were set from Refcyc being activated. In the circuit 300 which generates a refresh activation signal / REFE, it is inputted into NAND gate 302, and through the direct inverter 304, the output signal is inputted into NAND gate 308 through a delay circuit 306, and, as for both the flag Refflag set by the refresh flag generating circuit 100 from Refcyc, and Refwin generated from the refresh period generating circuit 200, outputs a refresh start signal / REFS. This signal is outputted as a refresh activation signal / REFE through a flip-flop 310. Refresh actuation is carried out according to the output of a refresh activation signal / REFE. After it is reversed with an inverter 312 and a refresh activation signal / REFE is delayed by part for a refresh actuation period, and the delay circuit 314, it is inputted into a flip-flop 310 and reset after predetermined time.

[0057] In the burst refresh control circuit 400, automatic detection of the long cycle is carried out, and burst refresh is set. For automatic detection of a long cycle, while Refflag is being activated, the reversal signal of Refcyc1 is outputted by (Refflag="H") and the AND gate 402, and it counts with a counter 404. If a counter 404 counts twice or more, since it will be detected as it being a long cycle, a flip-flop 406 is set and a long cycle signal / LONGCYCLE is outputted. And thereby, the refresh period signal Refwin is activated and burst refresh is performed. On the other hand, a flip-flop 406 is reset by the /ATD signal.

[0058]

[Effect of the Invention] In the semiconductor memory concerning this invention a refresh activation circuit Refresh actuation will be performed, if refresh actuation is attained after the 1st refresh cycle is generated by the 1st refresh cycle generating circuit. And when period refresh actuation longer than the 1st refresh cycle generated by the 1st refresh cycle generating circuit has not been carried out, It collects at the time within the long period (long cycle) of termination of the long period, and refresh actuation is continuously carried out based on the 2nd refresh cycle generated by the 2nd refresh cycle generating circuit. Therefore, the actuation to stability is attained, without being a high-speed cycle, and performing refresh actuation automatically in a long cycle at a need period, and the long cycle of the 1st more than refresh cycle time also destroying data, when it is not a long cycle (when rapid access being required).

[0059] In the aforementioned semiconductor memory, the aforementioned refresh activation circuit is preferably equipped with the detecting circuit which detects having not carried out period refresh actuation still longer than the 1st refresh cycle. Thereby, the automatic recognition of the long period can be carried out. Moreover, it is preferably detected as the aforementioned detecting circuit being the aforementioned long period, when it has the counter which counts the 1st refresh cycle in the condition that refresh actuation is demanded and a counter counts the 1st refresh cycle more than the count of predetermined. The automatic recognition of the long period can be carried out with an easy configuration.

[0060] In the semiconductor memory with which the interior low system actuation of a memory cell array is started in response to an external output enable signal or an external write enable signal For example, as for a refresh activation circuit, a period active state with long external output enable signal or external write enable signal continues. When period refresh actuation longer than the 1st refresh cycle generated by the 1st refresh cycle generating circuit has not been carried out, An external output enable signal or an external write enable signal will be in a non-active state. The refresh actuation based on the 1st refresh cycle is summarized by **********, and burst refresh is carried out based on the 2nd refresh cycle at the period when internal low system actuation becomes non-activity. Thereby, burst refresh can be performed in the semiconductor memory with which internal low system actuation is started in response to an external output enable signal or an external write enable signal.

[0061] The 2nd refresh cycle generating circuit generates a refresh cycle, when period refresh actuation longer than the 1st refresh cycle time generated by the 1st refresh cycle generating circuit has not been carried out, and refresh actuation is carried out. Thereby, the 2nd refresh generating circuit operates, only when required.

[0062] In the semiconductor memory of an address trigger mold for example, a refresh activation circuit When period refresh actuation longer than the 1st refresh cycle time which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit has not been carried out, An external output enable signal or an external write enable signal will be in a non-active state. The refresh actuation based on the 1st refresh cycle is summarized by **********, and burst refresh is carried out based on the 2nd refresh cycle at the period when internal low system actuation becomes non-activity. Thereby, internal low system actuation is started in response to an external address change. Thereby in a semiconductor memory, burst refresh can be performed.

[0063] In the aforementioned semiconductor memory, preferably, the condition that the address does not change continues, and a refresh activation circuit will stop internal low system actuation, if an external

output enable signal or an external write enable signal will be in a non-active state when period refresh actuation longer than the 1st refresh cycle generated by the 1st refresh cycle generating circuit has not been carried out. Thereby, burst refresh can be performed early.

[0064] In the aforementioned semiconductor memory preferably When the refresh activation circuit has not carried out period refresh actuation longer than the 1st refresh cycle which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit, If an external output enable signal or an external write enable signal will be in a non-active state After summarizing the refresh actuation based on the 1st refresh cycle by **********, carrying out refresh actuation based on the 2nd refresh cycle and ending by the count, re-activity of the low system actuation is carried out based on this. Thereby, the rapid access of degree cycle is realizable.

[0065] In the semiconductor memory of an address trigger mold, when the condition that the address is long and of not carrying out period change continues, after the condition has been recognized, a refresh activation circuit summarizes the refresh actuation based on the 1st refresh cycle by ********** based on address change of degree cycle, and carries out refresh actuation based on the 2nd refresh cycle. The limit of the period of /OE="H" after a long period is lost by this, and the degree of freedom of external timing goes up.

[0066] In the aforementioned semiconductor memory, preferably, the aforementioned refresh activation circuit does not carry out the aforementioned refresh actuation collectively carried out based on the 2nd refresh cycle, when an external output enable signal or an external write enable signal is activated after inactivation more quickly than a predetermined period. Since this does not perform burst refresh in a sudden long cycle, the problem that big access delay occurs is avoidable.

[0067] In the semiconductor memory of an address trigger mold for example, a refresh activation circuit When period refresh actuation longer than the 1st refresh cycle which the condition that the address does not change continues and is generated by the 1st refresh cycle generating circuit has not been carried out, After making low system actuation deactivate, summarizing the refresh actuation based on the 1st refresh cycle by **********, carrying out refresh actuation based on the 2nd refresh cycle and ending the refresh actuation for the count further, re-activity of the low system actuation is carried out. The limit of the period of /OE="H" after a long period is lost by this, and the degree of freedom of external timing goes up.

[Translation done.]

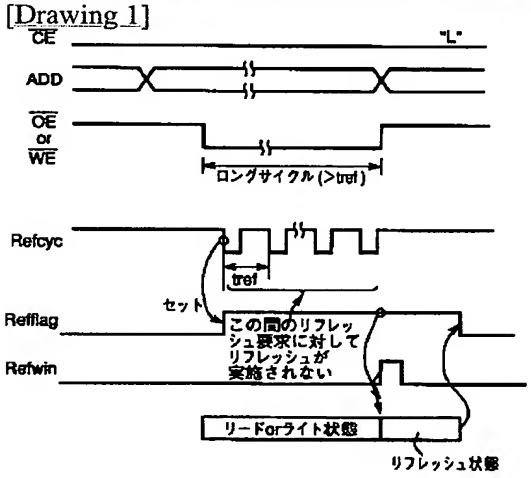
* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.

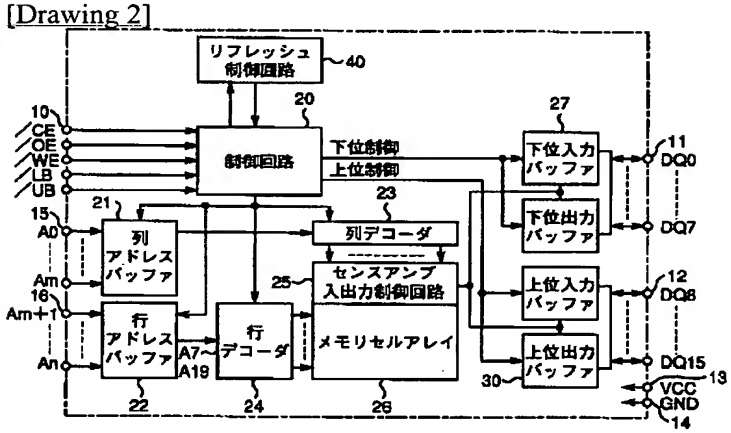
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

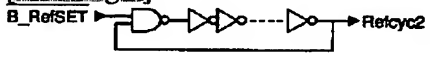
[Drawing 1]



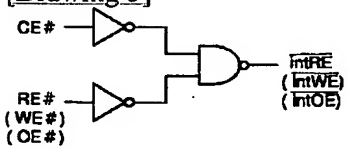
[Drawing 2]



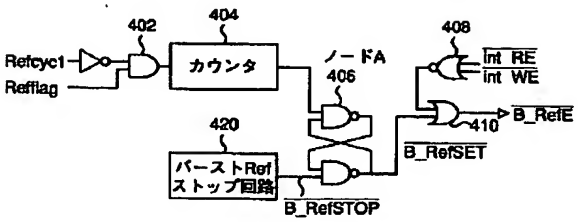
[Drawing 4]



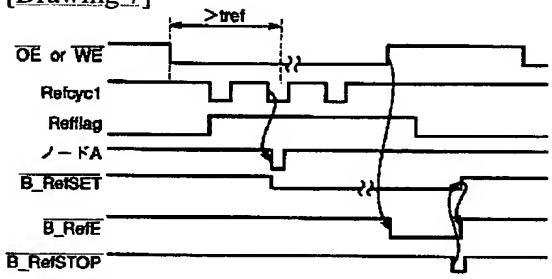
[Drawing 5]



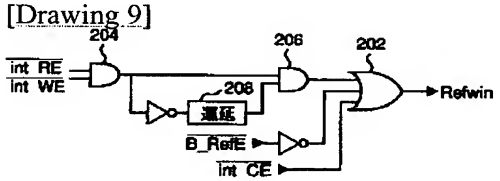
[Drawing 6]



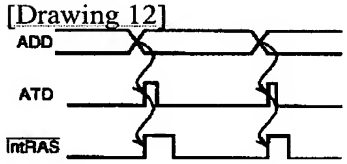
[Drawing 7]



[Drawing 9]



[Drawing 12]



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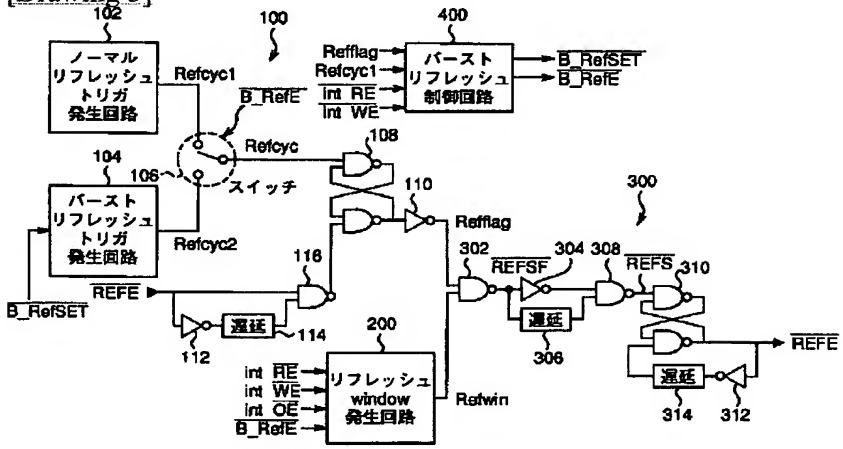
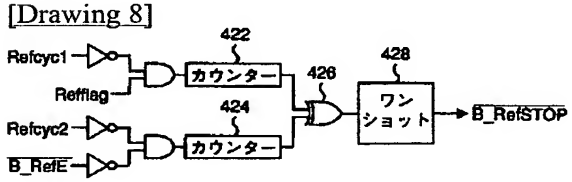
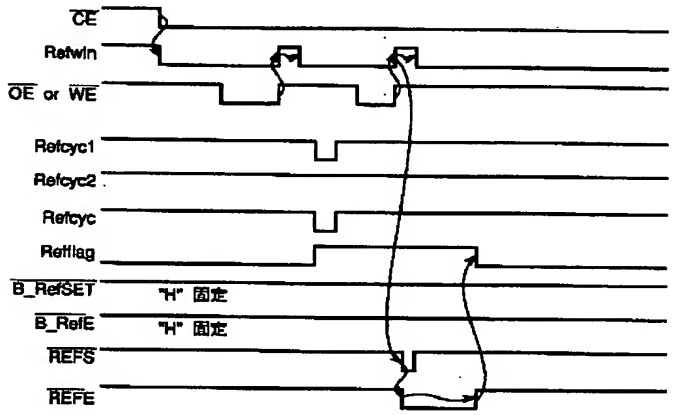


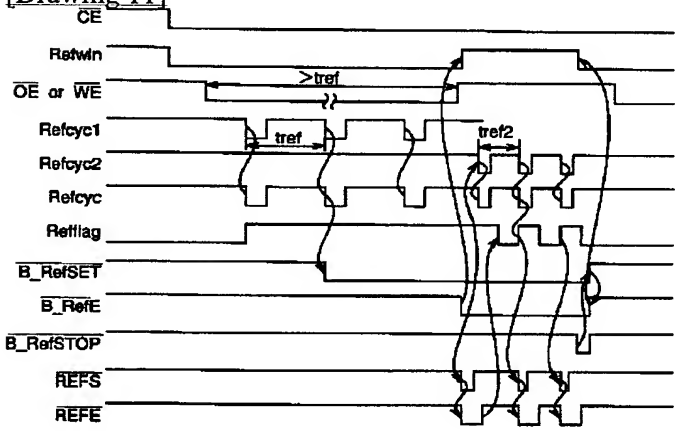
[Drawing 8]



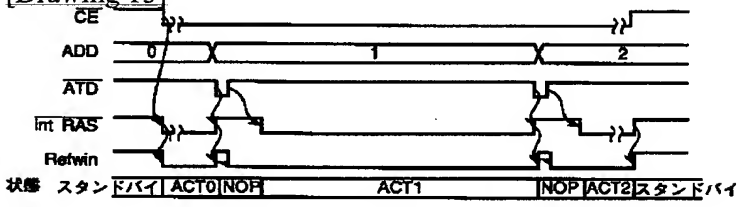
[Drawing 10]



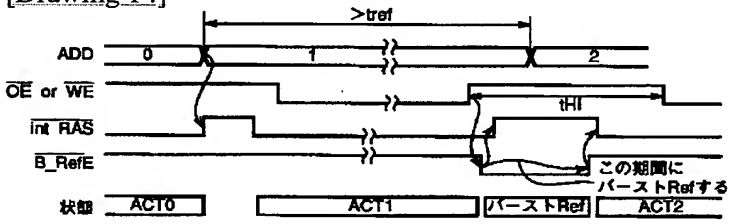
[Drawing 11]



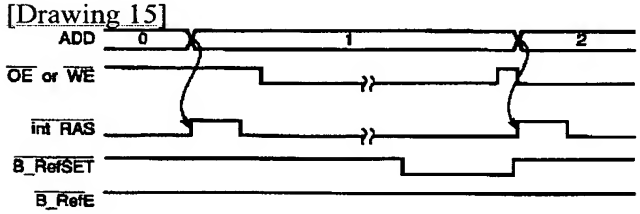
[Drawing 13]



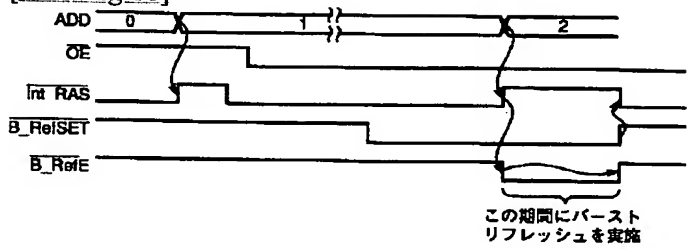
[Drawing 14]



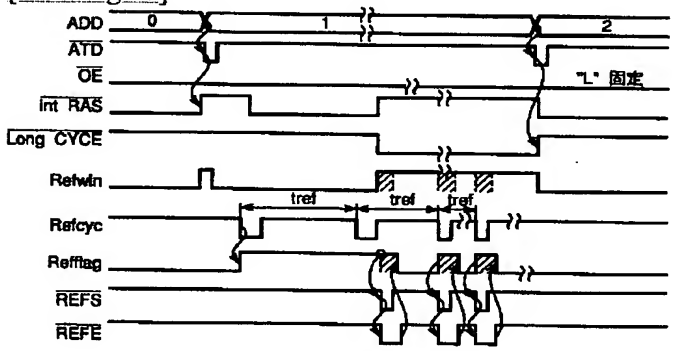
[Drawing 15]



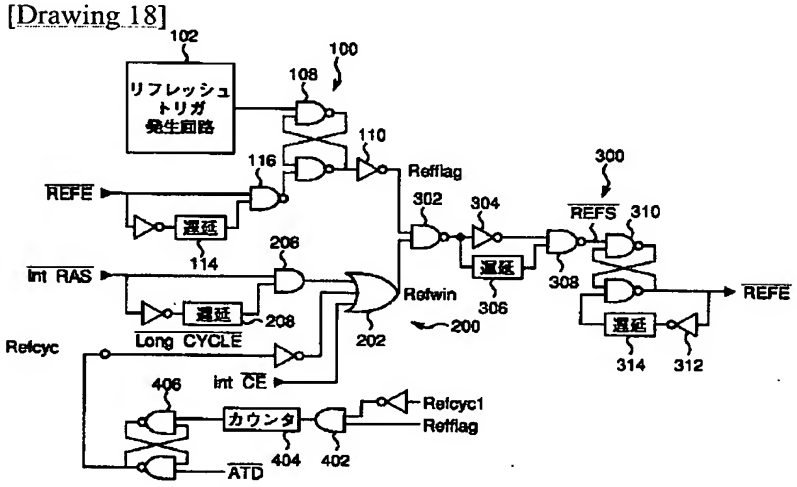
[Drawing 16]



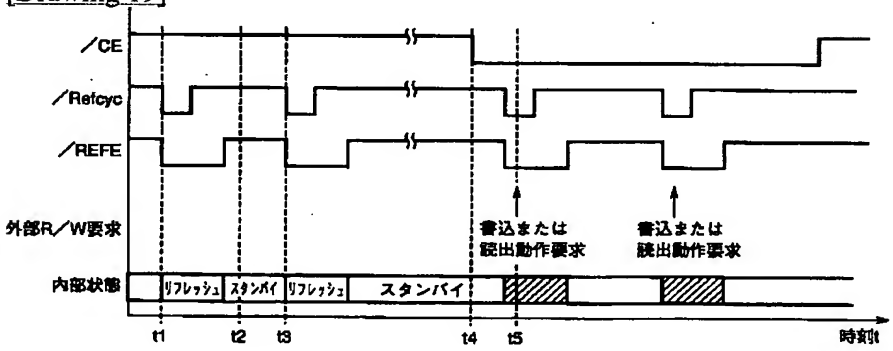
[Drawing 17]



[Drawing 18]



[Drawing 19]



[Translation done.]